LVC Series



What are ALVC & LVC logic families?

INTRODUCTION IDT's ALVC and LVC logic families are high performance bus inter- face components intended for low voltage applications. These components are fully compatible with industry standard components with similar designations, and they are specified for both 3.3V and 2.5V operation.

What are LVC logic devices?

LVC logic devices are specified over 1.65 V to 3.6 V(standard) or 1.65 V to 5.5 V (PicoGate). With a balanced output drive of 24 mA and typical propagation delay of 4 ns,the LVC family includes buffers/line drivers,transceivers,gates,analog switches and translators.

What are the features of LVC devices?

Over voltage tolerant I/O, source termination resistor, bus hold and power OFF are some of the advanced features of these devices making them ideal for parallel interface applications. LVC products are available in SO,TSSOP, PicoGate and innovative leadless MicroPak and DQFN packages for PCB space saving.

Is LVC a 5V tolerant logic device?

Lately, there has been much interest in LVC, the 5-V tolerant logic device family designed for medium performance needs (speed = 6.5 ns and drive = 24 mA). This designer's guide was created to answer customers' questions. Section 1 contains general characterization information about LVC.

What information does Ti provide about LVC?

Section 1 contains general characterization information about LVC. Section 2 contains data from direct-comparison tests conducted by TI's Advanced System Logic group. Appendices A-E include complete listings of the fully 5-V tolerant LVC device family, a list of frequently asked questions, and packaging information.

What is the difference between LVC and LVT?

LVC is a medium-speed logic family with a medium-drive capability. Additionally, the output drive of 64 mA for the LVT family is due to the bipolar circuitry in its output stage. Only LVC and LVT are 5-V tolerant. Figure D-1. Low-Voltage Product Positioning Table D-1 provides a further comparison of specific family features. Table D-1.

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